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PATENT APPLICATION

LIMITED THERMAL BUDGET FORMATION OF PMD LAYERS

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CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of and claims the benefit of co-pending, commonly assigned U.S. Patent Application No. 10/247,672, entitled, "METHOD USING TEOS RAMP-UP DURING TEOS/OZONE CVD FOR IMPROVED GAP FILL," filed on September 19, 2002, by Nitin K. Ingle, *et al.*, the entire disclosure of which is herein incorporated by reference for all purposes.

BACKGROUND OF THE INVENTION

[0002] The fabrication sequence of integrated circuits often includes several patterning processes. The patterning processes may define a layer of conductors, such as a patterned metal or polysilicon layer, or may define isolation structures, such as trenches. In many cases the trenches are filled with an insulating, or dielectric, material. This insulating material can serve several functions. For example, in some applications the material serves to both electrically isolate one region of the IC from another, and electrically passivate the surface of the trench. The material also typically provides a base for the next layer of the semiconductor structure to be built upon.

[0003] As semiconductor design has advanced, the feature size of semiconductor devices has dramatically decreased. Many circuits now have features, such as traces or trenches, less than a micron across. While the reduction in feature size has allowed higher device density, more chips per wafer, more complex circuits, lower operating power consumption and lower cost, among other benefits, the smaller geometries have also given rise to new problems, or have resurrected problems that were once solved for larger geometries.

[0004] An example of the type of manufacturing challenge presented by sub-micron devices is the ability to completely fill a narrow trench in a void-free manner. To fill a trench with silicon oxide, a layer of silicon oxide is first deposited on the patterned substrate. The silicon oxide layer typically covers the field, as well as walls and bottom of the trench. If the trench is wide and shallow, it is relatively easy to completely fill the trench. As the trench

gets narrower and the aspect ratio (the ratio of the trench height to the trench width) increases, it becomes more likely that the opening of the trench will "pinch off".

[0005] Pinching off a trench may trap a void within the trench. Voids resulting from pinching-off are undesirable as they can reduce the yield of good chips per wafer and the reliability of the devices. Under certain conditions, the void will be filled during a reflow process, for example where the deposited silicon oxide is doped and experiences viscous flow at elevated temperatures. However, as the trench becomes narrower, it becomes more likely that the void will not be filled during the reflow process. Moreover, several types of applications call for the deposition of undoped silicon oxide, which is difficult to reflow even at elevated temperature.

[0006] One possible solution to this problem is to anneal the oxide layer at high temperatures. Although successful in the past, this solution is no longer applicable in certain situations. New materials, such as nickel silicide, used in advanced semiconductor designs, have lowered thermal budgets, thus rendering some temperature/duration ranges of annealing unfeasible.

[0007] Therefore, it is desirable to be able to fill narrow gaps with dielectric material in a void-free manner. It is also desirable to do so without exceeding a thermal budget.

BRIEF SUMMARY OF THE INVENTION

[0008] Embodiments of the invention thus provide a method of filling a gap defined by adjacent raised features on a substrate. The method includes providing a flow of a silicon-containing processing gas to a chamber housing the substrate, providing a flow of an oxidizing processing gas to the chamber, and providing a flow of a phosphorous-containing processing gas to the chamber. The method also includes depositing a first portion of a P-doped silicon oxide film as a substantially conformal layer in the gap by causing a reaction between the silicon-containing processing gas, the phosphorous-containing processing gas, and the oxidizing processing gas. Depositing the conformal layer includes varying over time a ratio of the (silicon-containing processing gas plus phosphorous-containing processing gas):(oxidizing processing gas) and maintaining the temperature of the substrate below about 500°C throughout deposition of the conformal layer. The method also includes depositing a second portion of the P-doped silicon oxide film as a bulk layer. Depositing a second portion of the film includes maintaining the ratio of the (silicon-containing processing gas plus phosphorous-containing processing gas):(oxidizing processing gas) substantially constant

throughout deposition of the bulk layer and maintaining the temperature of the substrate below about 500°C throughout deposition of the bulk layer. In some embodiments, the method includes patterning metal lines on the substrate over the P-doped silicon oxide layer and maintaining the temperature of the substrate below a reflow temperature of the P-doped silicon oxide layer from a point in time immediately after deposition of the bulk layer to a point in time after patterning metal lines on the substrate.

[0009] In other embodiments, a method of filling a gap defined by adjacent raised features on a substrate includes providing a flow of a silicon-containing processing gas to a chamber housing the substrate and providing a flow of an oxidizing processing gas to the chamber. The method also includes depositing a first portion of a silicon oxide film as a substantially conformal layer in the gap by causing a reaction between the silicon-containing processing gas and the oxidizing processing gas. Depositing the conformal layer includes varying over time a ratio of the (silicon-containing processing gas):(oxidizing processing gas). The method also includes maintaining the temperature of the substrate below about 500°C throughout deposition of the conformal layer. The method also includes depositing a second portion of the silicon oxide film as a bulk layer. Depositing a second portion of the film includes maintaining the ratio of the (silicon-containing processing gas):(oxidizing processing gas) substantially constant throughout deposition of the bulk layer and maintaining the temperature of the substrate below about 500°C throughout deposition of the bulk layer. The method also includes depositing a cap layer comprising a P-doped silicon oxide film while maintaining the substrate below about 500°C throughout deposition of the cap layer.

[0010] In additional embodiments, a method is provided for processing a semiconductor substrate. The method includes providing a flow of a silicon-containing process gas to a chamber housing the substrate and providing a flow of an oxidizer process gas to the chamber. The method also includes causing a reaction between the silicon-containing process gas and the oxidizing process gas to form a silicon oxide layer on the substrate. The method further includes varying over time a ratio of the (silicon-containing gas):(oxidizing gas) flowed into the chamber to alter a rate of deposition of the silicon oxide on the substrate. During the process, the temperature of the substrate is maintained at or below a reflow temperature of the silicon oxide layer.

[0011] In some embodiments the silicon oxide layer may be a pre-metal dielectric layer. The substrate may include nickel silicide. The method may include providing a flow of a phosphorous-containing process gas to the chamber during a time period. The flow of silicon-containing process gas is provided at least partly during the time period. The silicon-containing process gas may include TEOS and the phosphorous-containing process gas may include TEPo.

[0012] In some embodiments the method includes thereafter providing a subsequent flow of phosphorous-containing process gas to the chamber. The method also may include, while providing the subsequent flow of phosphorous-containing process gas to the chamber, regulating a pressure of the chamber to a pressure in a range from about 200 torr to about 760 torr. The method also may include, while providing the subsequent flow of phosphorous-containing process gas to the chamber, forming a plasma from the phosphorous-containing process gas. The plasma may have a density greater than about 10^{11} ions/cm^3.

[0013] In still other embodiments, a method of processing a semiconductor substrate includes providing a flow of a silicon-containing process gas to a chamber housing the substrate, providing a flow of an oxidizing process gas to the chamber, and providing a flow of a phosphorous-containing process gas to the chamber. The method also includes causing a reaction between the silicon-containing process gas, the oxidizing process gas, and the phosphorous-containing gas to form a P-doped silicon oxide layer on the substrate. The method also includes varying over time a ratio of the (silicon-containing gas):(oxidizing gas):(phosphorous-containing gas) flowed into the chamber to alter a rate of deposition of the silicon oxide on the substrate. During the process, the temperature of the substrate is maintained at or below a temperature of 500°C.

[0014] In some embodiments, the P-doped silicon oxide layer comprises a pre-metal dielectric layer. The substrate may include nickel silicide. The silicon-containing process gas may include TEOS and the phosphorous-containing process gas may include TEPo.

[0015] In still other embodiments the method includes thereafter providing a subsequent flow of phosphorous-containing process gas to the chamber. The method may include, while providing the subsequent flow of phosphorous-containing process gas to the chamber, regulating a pressure of the chamber to a pressure in a range from about 200 torr to about 760 torr. The method also may include, while providing the subsequent flow of phosphorous-

containing process gas to the chamber, forming a plasma from the phosphorous-containing process gas. The plasma may have a density greater than about 10^{11} ions/cm^3.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the drawings wherein like reference numerals are used throughout the several drawings to refer to similar components.

[0017] Fig. 1 shows a simplified cross-sectional view of a trench filled with oxide utilizing conventional deposition techniques.

[0018] Fig. 2 shows a simplified cross-sectional view of an oxide-filled trench in accordance with embodiments of the present invention.

[0019] Fig. 3 illustrates a first deposition process according to embodiments of the invention.

[0020] Fig. 4 illustrates a second deposition process according to embodiments of the invention.

[0021] Fig. 5A is a simplified representation of a CVD apparatus according to an embodiment of the present invention.

[0022] Fig. 5B is a simplified representation of the user interface for a CVD system in relation to a deposition chamber in a multi-chamber system.

[0023] Fig. 5C is a simplified diagram of a gas panel and supply lines in relation to a deposition chamber.

[0024] Fig. 6 is a simplified cross section of a portion of an integrated circuit according to embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0025] Embodiments of the present invention provide methods, apparatuses, and devices related to chemical vapor deposition of silicon oxide particularly suitable for the formation of pre-metal dielectric (PMD) layers. In one embodiment, a process is used to form an undoped silicon oxide (sometimes referred to a undoped silicate glass, "USG") conformal layer followed by a P-doped silicon oxide (sometimes referred to as P-doped silicate glass, "PSG")

cap layer. During a first chemical vapor deposition (CVD) phase, silicon-containing gas and oxidizer gas are flowed while varying the ratio of the two, resulting in the formation of silicon oxide exhibiting a highly conformal character with good gap-filling properties. The PSG is then formed in a subsequent CVD phase. In other embodiments, a PSG conformal layer is formed by varying a ratio of (silicon-containing process gas):(phosphorous-containing process gas):(oxidizing process gas). In some such embodiments, a PSG cap layer may not be included. In both embodiments, however, the layers do not require an anneal process, thus avoiding steps that may risk exceeding a thermal budget. Aspects of the present invention are best understood with reference to the limitations of conventional processes.

I. Introduction

[0026] Fig. 1 shows a simplified cross-sectional view of an example of trench 100 filled with silicon oxide 102 deposited utilizing a conventional process. Fig. 1 shows that the increased rate of deposition of oxide material on the raised edges of the trench 100 has resulted in pinching-off of the trench and created unwanted void or pinhole defect 104 within the feature. Void 104 can adversely affect the operation of a semiconductor device that is relying upon the consistent dielectric strength of the oxide-filled trench.

[0027] The oxide-filled trench 100 may form part of a PMD structure. Traditionally, boron- and phosphorous-doped silicate glass (BPSG) formed in a sub-atmospheric chemical vapor deposition (SACVD) process has been used for PMD. Such films, however, typically require a high temperature anneal that takes the oxide beyond a glass transition temperature and allows it to reflow, thus removing voids, in most cases. The use of modern materials, such as nickel silicide, are incompatible with high temperature anneal processes as their inclusion in an integrated circuit may require that the substrate upon which the circuit is fabricated not be subjected to temperatures above 500°C.

[0028] Fig. 1 is to be contrasted with Fig. 2, which shows a simplified cross-sectional view of a trench structure 200 having an oxide layer 202 formed utilizing a process in accordance with an embodiment of the invention. In some embodiments, the oxide-filled trench is part of a PMD structure. The oxide layer may comprise a conformal layer 204 and a cap layer 206. The conformal layer 204 may comprise an undoped oxide or a P-doped oxide. In some embodiments, the conformal layer 204 may be formed by varying a ratio of (silicon-containing process gas):(oxidizing process gas), as will be described in more detail hereinafter. In some embodiments, the conformal layer is formed by varying a ratio of

(silicon-containing process gas):(phosphorous-containing process gas):(oxidizing process gas). The cap layer 206 may comprise PSG as a gettering layer. The PSG may be formed in a SACVD PSG process, a plasma-enhanced CVD (PECVD) PSG process, a high density CVD (HDCVD) PSG process, or similar process, as will be described hereinafter. In a specific embodiment relating to PMD, the conformal layer 204 comprises a P-doped oxide, and the cap layer is not be included.

[0029] The oxide-filled trench 200 of Fig. 2 does not include voids or weak seams associated with similar features formed utilizing conventional processes. Moreover, the oxide-filled trench 200 is formed without compromising a thermal budget.

II. Exemplary Deposition Processes

[0030] Having described embodiments of the invention generally, attention is directed to Fig. 3, which illustrates a first deposition process 300 according to an embodiment of the invention. The process 300 may be used to deposit a PMD or other layer. The process may take place in a CVD chamber, one example of which will be described hereinafter. The process 300 comprises conformal layer deposition 302 and cap layer deposition 304. In some embodiments, metal lines are patterned over the cap layer at block 305.

[0031] In a specific embodiment, the silicon-containing process gas comprises tetraethylorthosilicate (TEOS); however, other silicon-containing process gases such as SiH_4, S_2H_6, S_3H_8, etc., may be used. Also in a specific embodiment, the oxidizing process gas comprises ozone (O_3), although oxidizing gases such as O_2, H_2O, H_2O_2 may alternatively be used. Furthermore, this embodiment of the invention is described for gapfill using USG, but it will be appreciated that in alternative embodiments the film may be doped, as will be described below with reference to Fig. 4.

[0032] Conformal layer deposition 302 may be performed according to the process described in more detail in previously-incorporated U.S. Patent Application No. 10/247,672. The process includes flowing a silicon-containing process gas 306 and an oxidizing process gas 308. The ratio (silicon-containing gas):(oxidizer-containing gas) is varied 310, thereby varying the rate at which the conformal layer is deposited and possibly the composition of the conformal layer. For example, at the start of the process the concentration of the silicon-containing gas in the mixture may be small, then may be increased as the film thickness increases. In such examples, conformal layer deposition 302 may comprise depositing a conformal layer during a phase in which the silicon-containing gas concentration in the

mixture is small, then depositing a bulk layer during a phase in which the silicon-containing gas concentration in the mixture is higher.

[0033] The temperature of the substrate is regulated 312, in some cases in both degree and duration, such that a thermal budget is not exceeded. Regulating the temperature 312 may take place during conformal layer deposition 302, cap layer deposition 304, and/or patterning metal lines 305. In some embodiments, this comprises maintaining the temperature below about 500°C throughout processing of the substrate. In some embodiments this comprises not annealing any layer of the substrate.

[0034] Cap layer deposition 304 may take place *in situ*. For example, if conformal layer deposition 302 takes place in a CVD chamber, then cap layer deposition 304 may take place in the same chamber immediately thereafter. Cap layer deposition 304 alternatively may take place *ex situ* by forming the cap layer in another chamber of a multi-chamber system or by forming it in a different chamber system. Cap layer deposition 302 comprises flowing a phosphorous-containing gas 314. In some embodiments, the phosphorous-containing gas comprises triethylphosphate (TEPo) or PH_3. Cap layer deposition 304 also may include flowing a silicon-containing process gas and an oxidizing process gas as described above for conformal layer deposition 302.

[0035] Cap layer deposition 304 also may include regulating the pressure of the deposition environment 316, and/or forming a plasma in the environment 318. In some embodiments, the plasma environment is a high density plasma environment, which is defined as having an ion intensity greater than 10^{11} ions/cm^3. The phosphorous concentration during cap layer deposition may range from about 7% to about 9% by weight in some embodiments and from about 3.5 to 4% by weight in other embodiments. Other embodiments comprise phosphorous concentrations in the range from about 1% to about 10% by weight. As stated above, cap layer deposition may include regulating the temperature of the substrate 320.

[0036] Fig. 4 illustrates a second deposition process 400 according to an embodiment of the invention. The process may be used, for example, to deposit a PSG PMD layer on a substrate. The process includes conformal layer deposition 402 and may include cap layer deposition 404. The process also may include patterning metal lines 405.

[0037] Conformal layer deposition 402 includes providing a silicon-containing process gas 406, an oxidizing process gas 408, and a phosphorous-containing process gas 410. The silicon-containing process gas may comprises tetraethylorthosilicate (TEOS) or other silicon-

containing gases, such as SiH_4, S_2H_6, S_3H_8. The oxidizing process gas may comprises ozone (O_3), O_2, H_2O, H_2O_2, or the like. In a specific embodiment, the phosphorous-containing gas comprises TEPo. Although this embodiment relates to depositing a P-doped conformal layer, additional dopants also may be used. For example, a flow of SiF_4 may be used to fluorinate the film, a flow of PH_3 may be used to phosphorate the film, a flow of B_2H_6 may be used to boronate the film, a flow of N_2 may be used to nitrogenate the film, and the like.

[0038] As described in more detail with respect to conformal layer deposition 302 above, the ratio of the three gases may be varied 412 to regulate the rate of deposition, for example, by maintaining the oxidizing process gas at a higher concentration at the beginning of the process and lowering the concentration of the oxidizing process gas as the film thickness increases. This may be accomplished by either decreasing the flow rate of the oxidizing process gas and/or increasing the flow rate of the other gases. The concentrations of the silicon-containing gas and/or the dopant gas may be similarly regulated.

[0039] The temperature also may be regulated 414 in both degree and duration such that a thermal budget is not exceeded. As described above, regulating the temperature 414 may take place during conformal layer deposition 402, cap layer deposition 404, and/or patterning metal lines 405. In some embodiments, this comprises maintaining the temperature below about 500°C throughout processing of the substrate. In some embodiments this comprises not annealing any layer of the substrate. If desired, cap layer deposition 404 proceeds as previously described for cap layer deposition 304 of Fig. 3, which includes providing a phosphorous-containing gas 416, regulating the pressure 418, in some embodiments forming a plasma 420, and regulating the temperature 422.

[0040] The deposition steps 302, 304, 402, 404 may comprise an SACVD process. In such a process, while the temperature profile may be regulated so as to remain within a thermal budget, it should be noted that the gapfill process tends to be more successful at higher temperatures. With high aspect ratio narrow gaps, greater success is achieved by varying the ratio (silicon-containing process gas):(oxidizing gas), beginning with a lower concentration of silicon-containing process gas, as described above and more fully in previously-incorporated U.S. Patent Application No. 10/247,672. The process may be further aided by disbursing the gas uniformly across the substrate. As the concentration of silicon-containing process gas in the mixture increases, the gas may be disbursed closer to the surface of the substrate. This technique and an apparatus for practicing it are more fully described in co-

pending, commonly assigned U.S. Patent Application No. 10/057,280, filed on January 25, 2002, entitled "GAS DISTRIBUTION SHOWERHEAD," and/or co-pending, commonly assigned U.S. Patent Application No. 10/674,569, filed on September 29, 2003, entitled "GAS DISTRIBUTION SHOWERHEAD," the entire disclosure of each of which are herein incorporated by reference. The combination of varying the processing gas ratios and disbursing the gases at varying distances from the wafer produce better gapfill that, in most cases, requires no annealing.

[0041] Alternative embodiments of the previously-described processes may include more or fewer operations. Further, the operations in alternative embodiments are not necessarily performed in the order depicted, as is apparent to those skilled in the art in light of the disclosure herein.

III. An Exemplary Deposition System

[0042] Having described methods according to embodiments of the present invention, attention is directed to Fig. 5A, which illustrates a simplified diagram of a CVD system 510 according to an embodiment of the present invention. This system is suitable for performing thermal, SACVD processes, as well as other processes, such as reflow, drive-in, cleaning, etching, and gettering processes. Multiple-step processes can also be performed on a single substrate or wafer without removing the substrate from the chamber. The major components of the system include, among others, a vacuum chamber 515 that receives process and other gases from a gas delivery system 589, a vacuum system 588, a remote microwave plasma system 555, and a control system 553. These and other components are described below in order to understand the present invention.

[0043] The CVD apparatus 510 includes an enclosure assembly 512 housing a vacuum chamber 515 with a gas reaction area 516. A gas distribution plate 520 is provided above the gas reaction area 516 for dispersing reactive gases and other gases, such as purge gases, through perforated holes in the gas distribution plate 520 to a wafer (not shown) that rests on a vertically movable heater 525 (also referred to as a wafer support pedestal). The heater 525 can be controllably moved between a lower position, where a wafer can be loaded or unloaded, for example, and a processing position closely adjacent to the gas distribution plate 520, indicated by a dashed line 513, or to other positions for other purposes, such as for an etch or cleaning process. A center board (not shown) includes sensors for providing information on the position of the wafer.

[0044] In some embodiments, the gas distribution plate 520 may be of the variety described in either of previously-incorporated U.S. Patent Application Serial Nos. 10/057,280 or 10/674,569. These plates improve the uniformity of gas disbursement at the substrate and are particularly advantageous in deposition processes that vary gas concentration ratios. In some examples, the plates work in combination with the vertically moveable heater 525 (or moveable wafer support pedestal) such that deposition gases are released farther from the substrate when the ratio is heavily skewed in one direction (*e.g.*, when the concentration of a silicon-containing gas is small compared to the concentration of an oxidizer-containing gas) and are released closer to the substrate as the concentration changes (*e.g.*, when the concentration of silicon-containing gas in the mixture is higher). In other examples, the orifices of the gas distribution plate are designed to provide more uniform mixing of the gases.

[0045] The heater 525 includes an electrically resistive heating element (not shown) enclosed in a ceramic. The ceramic protects the heating element from potentially corrosive chamber environments and allows the heater to attain temperatures up to about 800°C. In an exemplary embodiment, all surfaces of the heater 525 exposed to the vacuum chamber 515 are made of a ceramic material, such as aluminum oxide (Al_2O_3 or alumina) or aluminum nitride.

[0046] Reactive and carrier gases are supplied through the supply line 543 into a gas mixing box (also called a gas mixing block) 527, where they are preferably mixed together and delivered to the gas distribution plate 520. The gas mixing box 527 is preferably a dual input mixing block coupled to a process gas supply line 543 and to a cleaning/etch gas conduit 547. A valve 528 operates to admit or seal gas or plasma from the gas conduit 547 to the gas mixing block 527. The gas conduit 547 receives gases from an integral remote microwave plasma system 555, which has an inlet 557 for receiving input gases. During deposition processing, gas supplied to the plate 520 is vented toward the wafer surface (as indicated by arrows 521), where it may be uniformly distributed radially across the wafer surface, typically in a laminar flow.

[0047] Purging gas may be delivered into the vacuum chamber 515 from the plate 520 and/or an inlet port or tube (not shown) through the bottom wall of enclosure assembly 512. The purging gas flows upward from the inlet port past the heater 525 and to an annular pumping channel 540. An exhaust system then exhausts the gas (as indicated by arrows 522)

into the annular pumping channel 540 and through an exhaust line 560 to a vacuum system 588, which includes a vacuum pump (not shown). Exhaust gases and entrained particles are drawn from the annular pumping channel 540 through the exhaust line 560 at a rate controlled by a throttle valve system 563.

[0048] The remote microwave plasma system 555 can produce a plasma for selected applications, such as chamber cleaning or etching native oxide or residue from a process wafer. Plasma species produced in the remote plasma system 555 from precursors supplied via the input line 557 are sent via the conduit 547 for dispersion through the plate 520 to the vacuum chamber 515. Precursor gases for a cleaning application may include fluorine, chlorine, and other reactive elements. The remote microwave plasma system 555 also may be adapted to deposit plasma-enhanced CVD films by selecting appropriate deposition precursor gases for use in the remote microwave plasma system 555.

[0049] The system controller 553 controls activities and operating parameters of the deposition system. The processor 550 executes system control software, such as a computer program stored in a memory 570 coupled to the processor 550. Preferably, the memory 570 may be a hard disk drive, but of course the memory 570 may be other kinds of memory, such as read-only memory or flash memory. In addition to a hard disk drive (e.g., memory 570), the CVD apparatus 510 in a preferred embodiment includes a floppy disk drive and a card rack (not shown).

[0050] The processor 550 operates according to system control software programmed to operate the device according to the methods disclosed herein. For example, sets of instructions may dictate the timing, mixture of gases, chamber pressure, chamber temperature, microwave power levels, susceptor position, and other parameters of a particular process. Other computer programs such as those stored on other memory including, for example, a floppy disk or another computer program product inserted in a disk drive or other appropriate drive, may also be used to operate the processor 550 to configure the CVD system 510 into various apparatus.

[0051] The processor 550 has a card rack (not shown) that contains a single-board computer, analog and digital input/output boards, interface boards and stepper motor controller boards. Various parts of the CVD system 510 conform to the Versa Modular European (VME) standard which defines board, card cage, and connector dimensions and

types. The VME standard also defines the bus structure having a 16-bit data bus and 24-bit address bus.

[0052] Fig. 5B is a simplified diagram of a user interface in relation to the CVD apparatus chamber 530. The CVD apparatus 510 includes one chamber of a multichamber system. Wafers may be transferred from one chamber to another for additional processing. In some cases the wafers are transferred under vacuum or a selected gas. The interface between a user and the processor is via a CRT monitor 573a and a light pen 573b. A mainframe unit 575 provides electrical, plumbing, and other support functions for the CVD apparatus 510. Exemplary mainframe units compatible with the illustrative embodiment of the CVD apparatus are currently commercially available as the PRECISION 5000™, the CENTURA 5200™, and the PRODUCER SE™ systems from APPLIED MATERIALS, INC. of Santa Clara, California.

[0053] In some embodiments two monitors 573a are used, one mounted in the clean room wall 571 for the operators, and the other behind the wall 572 for the service technicians. Both monitors 573a simultaneously display the same information, but only one light pen 573b is enabled. The light pen 573b detects light emitted by the CRT display with a light sensor in the tip of the pen. To select a particular screen or function, the operator touches a designated area of the display screen and pushes the button on the pen 573b. The touched area changes its highlighted color, or a new menu or screen is displayed, confirming communication between the light pen and the display screen. Of course, other devices, such as a keyboard, mouse, or other pointing or communication device, may be used instead of or in addition to the light pen 573b to allow the user to communicate with the processor.

[0054] Fig. 5C illustrates a general overview of an embodiment of the CVD apparatus 510 in relation to a gas supply panel 580 located in a clean room. As discussed above, the CVD system 510 includes a chamber 515 with a heater 525, a gas mixing box 527 with inputs from an inlet tube 543 and a conduit 547, and remote microwave plasma system 555 with input line 557. As mentioned above, the gas mixing box 527 is for mixing and injecting deposition gas(es) and clean gas(es) or other gas(es) through the inlet tube 543 to the processing chamber 515.

[0055] The remote microwave plasma system 555 is integrally located and mounted below the chamber 515 with the conduit 547 coming up alongside the chamber 515 to the gate valve 528 and the gas mixing box 527, located above the chamber 515. Microwave generator 511

and ozonator 551 are located remote from the clean room. Supply lines 583 and 585 from the gas supply panel 580 provide reactive gases to the gas supply line 543. The gas supply panel 580 includes lines from gas or liquid sources 590 that provide the process gases for the selected application. The gas supply panel 580 has a mixing system 593 that mixes selected gases before flow to the gas mixing box 527. In some embodiments, gas mixing system 593 includes a liquid injection system for vaporizing reactant liquids such as tetraethylorthosilicate ("TEOS"), triethylborate ("TEB"), and triethylphosphate ("TEPO"). Vapor from the liquids is usually combined with a carrier gas, such as helium. Supply lines for the process gases may include (i) shut-off valves 595 that can be used to automatically or manually shut off the flow of process gas into line 585 or line 557, and (ii) liquid flow meters (LFM) 501 or other types of controllers that measure the flow of gas or liquid through the supply lines.

[0056] As an example, a mixture including TEOS as a silicon source may be used with gas mixing system 593 in a deposition process for forming a silicon oxide film. The TEPO is a liquid source that may be vaporized by conventional boiler-type or bubbler-type hot boxes. However, a liquid injection system is preferred as it provides greater control of the volume of reactant liquid introduced into the gas mixing system. The liquid is typically injected as a fine spray or mist into the carrier gas flow before being delivered to a heated gas delivery line 585 to the gas mixing block and chamber. One or more sources, such as oxygen (O_2) or ozone (O_3) flow to the chamber through another gas delivery line 583, to be combined with the reactant gases from heated gas delivery line 585 near or in the chamber. Of course, it is recognized that other sources of dopants, silicon, and oxygen also may be used.

IV. Exemplary Semiconductor Structure

[0057] Fig. 6 illustrates a simplified cross-sectional view of an integrated circuit 700 according to an embodiment of the present invention. As shown in Fig. 7, the integrated circuit 700 includes NMOS and PMOS transistors 703 and 706, which are separated and electrically isolated from each other by oxide-filled trench isolation structure 720. Alternatively, field oxide isolation can be used to isolate devices, or a combination of isolation techniques may be used. Each of the transistors 703 and 706 comprises a source region 712, a gate region 715, and a drain region 718.

[0058] A premetal dielectric (PMD) layer 721 separates the transistors 703 and 706 from the metal layer 740, with connections between metal layer 740 and the transistors made by

contacts 724. The premetal dielectric layer 721 may comprise a single layer or multiple layers. The metal layer 740 is one of four metal layers, 740, 742, 744, and 746, included in the integrated circuit 700. Each metal layer is separated from adjacent metal layers by intermetal dielectric layers 727, 728, and 729. Adjacent metal layers are connected at selected openings by vias 726. Planarized passivation layers 730 are deposited over the metal layer 746.

[0059] A silicon oxide layer deposited according to an embodiment of the present invention may be used to form one or more of the dielectric layers shown in integrated circuit 700. For example, a silicon oxide layer may be used to create trench isolation structure 720. A silicon oxide layer deposited according to the present invention may also be used to create PMD layer 721, or the higher layer intermetal dielectric layers 727-729 of the overlying interconnect structure.

[0060] A silicon oxide layer deposited according to an embodiment of the present invention may also be used in damascene layers, which are included in some integrated circuits. In damascene layers, a blanket layer is deposited over a substrate, selectively etched through to the substrate, and then filled with metal and etched back or polished to form metal contacts 724. After the metal layer is deposited, a second blanket deposition is performed and selectively etched. The etched areas are then filled with metal and etched back or polished to form vias 726.

[0061] It should be understood that the simplified integrated circuit 700 is for illustrative purposes only. One of ordinary skill in the art could implement the present method for fabrication of other integrated circuits, such as microprocessors, application-specific integrated circuits (ASICs), memory devices, and the like.

[0062] Having described several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the invention. For example, although embodiments of the present invention have been described with respect to depositing a PMD layer, other embodiments may be directed toward depositing other layers. Additionally, a number of well known processes and elements have not been described in order to avoid unnecessarily obscuring the present invention. Accordingly, the above description should not be taken as limiting the scope of the invention, which is defined in the following claims.